What is claimed is:

1. An apparatus, comprising:

an input block to apply an input signal to a common input terminal of a sensing block; and

a converting block to receive a sensed signal from the sensing block in response to applying the input signal.

2. The apparatus of claim 1, wherein the converting block provides an output signal based on the sensed signal.

3. The apparatus of claim 1, wherein the converting block provides a signal having a fractional pulse density that is indicative of acceleration.

4. The apparatus of claim 1, wherein the input block applies a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

5. The apparatus of claim 1, wherein the converting block integrates the sensed signal and provides a first output signal and a second output signal.

6. The apparatus of claim 5, wherein the converting block further compares the first output signal and the second output signal and provides an output signal.

7. The apparatus of claim 6, wherein the converting block provides the output signal to the input block.

8. The apparatus of claim 1, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block provides a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

9. The apparatus of claim 8, wherein the input block provides the first input signal through a first capacitor and the second input signal through a second capacitor.

10. The apparatus of claim 1, further comprising a storage unit to store one or more voltage values to apply to the apparatus.

11. A method comprising:

providing an input signal to a common input terminal of a sensing block;

receiving a sensed signal from the sensing block based on providing the input signal; and

providing a signal based on the sensed signal.

12. The method of claim 11, comprising providing a digital signal based on the sensed signal.

13. The method of claim 11, comprising providing signal having a fractional pulse density that is indicative of acceleration.

14. The method of claim 11, comprising providing a first signal to the common input terminal during a first clock phase and a second signal to the common input terminal during a second clock phase.

15. The method of claim 14, comprising providing the first signal and the second signal to the common input terminal during non-overlapping clock cycles.

16. The method of claim 15, comprising integrating the sensed signal and providing a first output signal and a second output signal.

17. The method of claim 16, comprising comparing the first output signal and the second output signal and provides an output signal.

18. The method of claim 17, comprising providing the first signal and second signal based at least in part on the output signal.

19. An apparatus, comprising:

an input block to provide an input signal to a common terminal of a first capacitor and a second capacitor of a sensing block; and

a converting block to receive a sensed signal from the sensing block in response to applying the input signal.

20. The apparatus of claim 19, wherein the converting block provides a digital signal based on the sensed signal.

21. The apparatus of claim 19, wherein the input block applies a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

22. The apparatus of claim 19, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block provides a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

23. The apparatus of claim 19, wherein the converting block comprises:

an integrator to receive the sensed signal from the sensing block and to produce an integrated signal;

a comparator to receive the integrated signal and to provide an output signal; and

a latch to receive the output signal and to provide a latched output signal.

24. The apparatus of claim 19, further comprising a storage unit to store one or more voltage values to apply to the sensing circuit.

25. A restraint system, comprising:

a sensing circuit to:

apply an input signal to a common input terminal of a sensing block;

receive a sensed signal from the sensing block in response to applying the input signal; and

provide an output signal based at least in part on the sensed signal; and

a deployment block to provide an activation signal based at least in part on the output signal from the sensing circuit.

26. The restraint system of claim 25, wherein the deployment block provides the activation signal to activate an airbag.

27. The restraint system of claim 25, wherein the sensing circuit is clocked using a plurality of non-overlapping clocks.

28. The restraint system of claim 25, wherein the sensing circuit provides a digital signal.

29. The restraint system of claim 25, wherein the sensing circuit provides a signal having a fractional pulse density that is indicative of acceleration.

30. The restraint system of claim 25, further comprising a storage unit to store one or more voltage values to apply to the sensing circuit.